# LH5164AVH

***PRELIMINARY***

**CMOS 64K (8K × 8) Static RAM**

## FEATURES

- 8,192 × 8 bit organization
- Access time: 200 ns (MAX.)
- Supply current (MAX.):
  - Operating: 90 mW
    - 29 mW ($t_{RC}$, $t_{WC}$ = 1 µs)
  - Standby: 3.6 µW (MAX.) @ 70°C
    - 10.8 µW (MAX.) @ 85°C
  - Data retention:
    - 0.6 µW ($V_{CC}$ = 3 V, $t_A$ = 25°C)
- Low voltage operation: 3.3 V ±0.3 V
- Fully-static operation
- TTL compatible I/O
- Three-state outputs
- Packages:
  - 28-pin, 450-mil SOP
  - 28-pin, 8 × 13 mm$^2$ TSOP (Type I)

## DESCRIPTION

The LH5164AVH is a static RAM organized as 8,192 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

## PIN CONNECTIONS

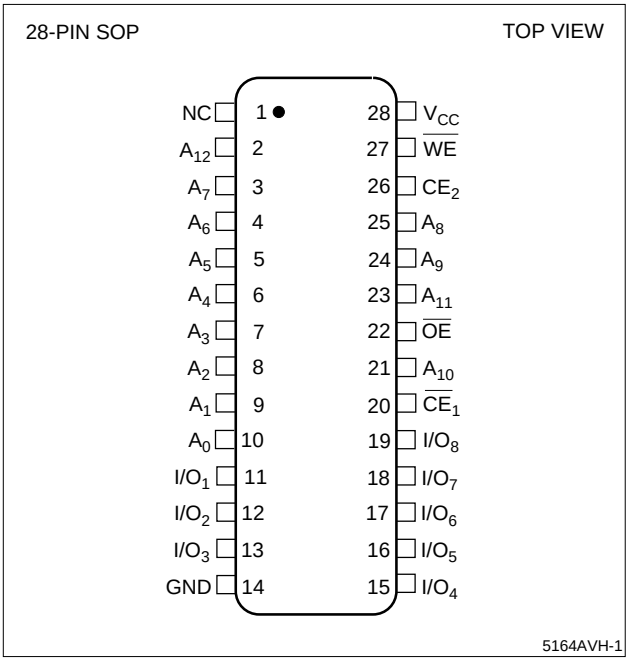



**Figure 1. Pin Connections for SOP Package**

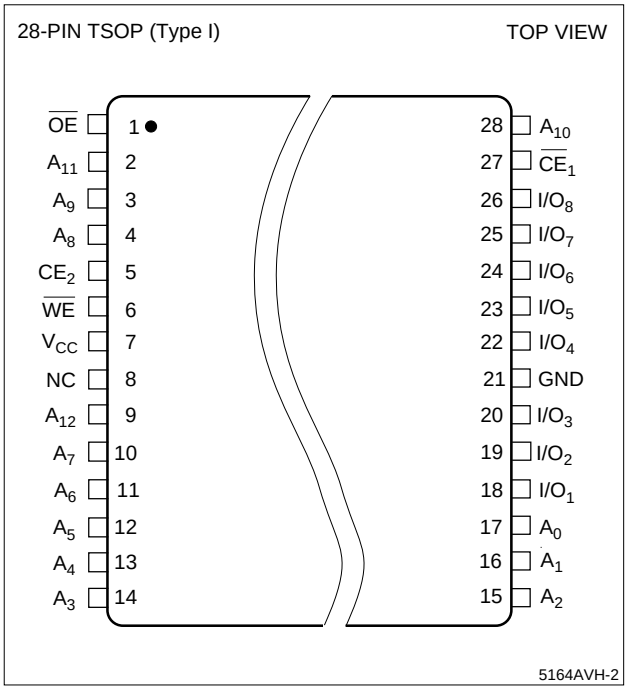



**Figure 2. Pin Connections for TSOP Package**

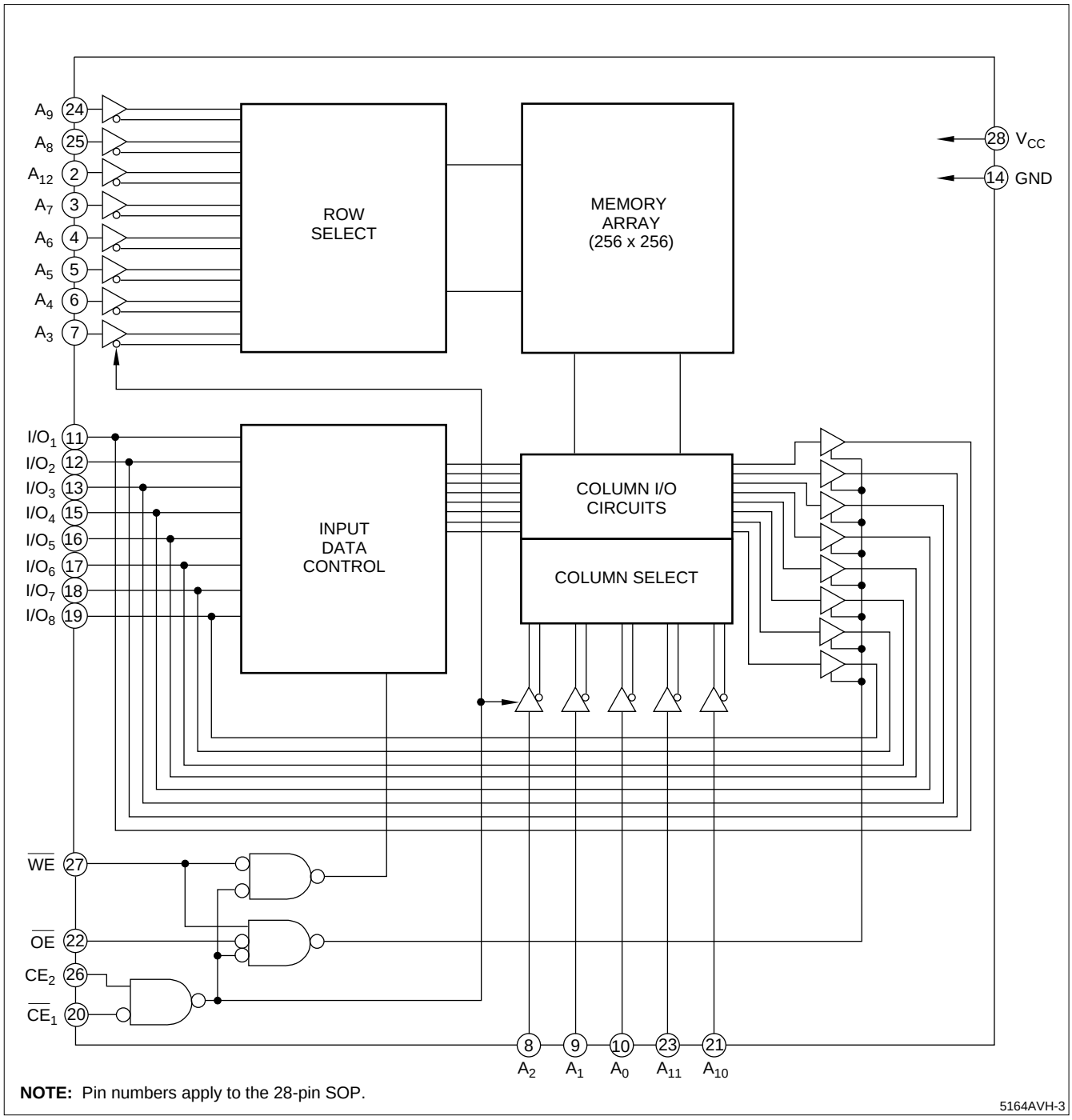



**Figure 3. LH5164AVH Block Diagram**

## PIN DESCRIPTION

| SIGNAL | PIN NAME |
|---|---|
| $A_0$ - $A_{12}$ | Address inputs |
| $\overline{CE}_1/CE_2$ | Chip Enable input |
| $\overline{WE}$ | Write Enable input |
| $\overline{OE}$ | Output Enable input |

| SIGNAL | PIN NAME |
|---|---|
| $I/O_1$ - $I/O_8$ | Data inputs and outputs |
| $V_{CC}$ | Power supply |
| GND | Ground |
| NC | No connection |

## TRUTH TABLE

| $\overline{CE_1}$ | $CE_2$ | $\overline{WE}$ | $\overline{OE}$ | MODE | $I/O_1$ - $I/O_8$ | SUPPLY CURRENT | NOTE |
|---|---|---|---|---|---|---|---|
| H | X | X | X | Standby | High-Z | Standby ($I_{SB}$) | 1 |
| X | L | X | X | | | | |
| L | H | L | X | Write | Data input | Operating ($I_{CC}$) | 1 |
| L | H | H | L | Read | Data output | Operating ($I_{CC}$) | |
| L | H | H | H | Output disable | High-Z | Operating ($I_{CC}$) | |

**NOTE:**
1. X = H or L

## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | SYMBOL | RATING | UNIT | NOTE |
|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | –0.3 to +7.0 | V | 1 |
| Input voltage | $V_{IN}$ | –0.3 to $V_{CC}$ +0.3 | V | 1, 2 |
| Operating temperature | Topr | –40 to +85 | °C | |
| Storage temperature | Tstg | –65 to +150 | °C | |

**NOTES:**
1. The maximum applicable voltage on any pin with respect to GND.
2. $V_{IN}$ (MIN.) = –3.0 V for pulse width ≤50 ns.

## RECOMMENDED OPERATING CONDITIONS ($T_A$ = –40°C to +85°C)

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT | NOTE |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | 3.0 | 3.3 | 3.6 | V | |
| Input voltage | $V_{IH}$ | $V_{CC}$ – 0.5 | | $V_{CC}$ + 0.3 | V | |
| | $V_{IL}$ | –0.3 | | 0.2 | V | 1 |

**NOTE:**
1. $V_{IL}$ (MIN.) = –3.0 V for pulse width ≤50 ns.

## DC CHARACTERISTICS [1] ($T_A$ = –40°C to +85°C, $V_{CC}$ = 3.3 V ±0.3 V)

| PARAMETER | SYMBOL | CONDITIONS | | MIN. | MAX. | UNIT | NOTE |
|---|---|---|---|---|---|---|---|
| Input leakage current | $I_{LI}$ | $V_{IN}$ = 0 V to $V_{CC}$ | | –1.0 | 1.0 | µA | |
| Output leakage current | $I_{LO}$ | $\overline{CE_1}$ = $V_{IH}$ or $CE_2$ = $V_{IL}$ or $\overline{OE}$ = $V_{IH}$ or $\overline{WE}$ = $V_{IL}$ $V_{I/O}$ = 0 to $V_{CC}$ | | –1.0 | 1.0 | µA | |
| Operating supply current | $I_{CC}$ | $\overline{CE_1}$ = 0.2 V, $V_{IN}$ = 0.2 V, or $V_{CC}$ – 0.2 V $CE_2$ = $V_{CC}$ – 0.2 V, Outputs open | $t_{CYCLE}$ = 200 ns | | 25 | mA | |
| | | | $t_{CYCLE}$ = 1.0 µs | | 8 | | |
| Standby current | $I_{SB}$ | $CE_2$ ≤ 0.2 V or $\overline{CE_1}$ ≥ $V_{CC}$ – 0.2 V | $T_A$ ≤ +70°C | | 1.0 | µA | 1 |
| | | | $T_A$ ≤ +85°C | | 3.0 | | |
| | $I_{SB1}$ | $\overline{CE_1}$ = $V_{IH}$ or $CE_2$ = $V_{IL}$ | | | 5 | mA | |
| Output voltage | $V_{OL}$ | $I_{OL}$ = 500 µA | | | 0.4 | V | |
| | $V_{OH}$ | $I_{OH}$ = –500 µA | | $V_{CC}$ – 0.5 | | V | |

**NOTE:**

1. $CE_2$ should be ≥ $V_{CC}$ – 0.2 V or ≤0.2 V when $\overline{CE_1}$ ≥ $V_{CC}$ – 0.2 V.

## READ CYCLE ($T_A$ = –40°C to +85°C, $V_{CC}$ = 3.3 V ±0.3 V)

| PARAMETER | SYMBOL | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| Read cycle time | $t_{RC}$ | 200 | | ns |
| Address access time | $t_{AA}$ | | 200 | ns |
| $\overline{CE}_1$ access time | $t_{ACE1}$ | | 200 | ns |
| $CE_2$ access time | $t_{ACE2}$ | | 200 | ns |
| Output enable access time | $t_{OE}$ | | 150 | ns |
| Output hold time | $t_{OH}$ | 10 | | ns |
| $\overline{CE}_1$ Low to output in Low-Z | $t_{LZ1}$ | 20 | | ns |
| $CE_2$ High to output in Low-Z | $t_{LZ2}$ | 20 | | ns |
| $\overline{OE}$ Low to output in Low-Z | $t_{OLZ}$ | 10 | | ns |
| $\overline{CE}_1$ High to output in High-Z | $t_{HZ1}$ | 0 | 60 | ns |
| $CE_2$ Low to output in High-Z | $t_{HZ2}$ | 0 | 60 | ns |
| $\overline{OE}$ High to output in High-Z | $t_{OHZ}$ | 0 | 40 | ns |

## WRITE CYCLE ($T_A$ = –40°C to +85°C, $V_{CC}$ = 3.3 V ±0.3 V)

| PARAMETER | SYMBOL | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| Write cycle time | $t_{WC}$ | 200 | | ns |
| $\overline{CE}$ Low to end of write | $t_{CW}$ | 180 | | ns |
| Address valid to end of write | $t_{AW}$ | 180 | | ns |
| Address setup time | $t_{AS}$ | 0 | | ns |
| Write pulse width | $t_{WP}$ | 150 | | ns |
| Write recovery time | $t_{WR}$ | 0 | | ns |
| Input data setup time | $t_{DW}$ | 100 | | ns |
| Input data hold time | $t_{DH}$ | 0 | | ns |
| $\overline{WE}$ High to output in Low-Z | $t_{OW}$ | 20 | | ns |
| $\overline{WE}$ Low to output in High-Z | $t_{WZ}$ | 0 | 60 | ns |
| $\overline{OE}$ High to output in High-Z | $t_{OHZ}$ | 0 | 40 | ns |

## TEST CONDITIONS

| PARAMETER | MODE | NOTE |
|---|---|---|
| Input pulse level | 0.2 V to $V_{CC}$ – 0.2 V | |
| Input rise/fall time | 10 ns | |
| Input/output timing level | 1.5 V | |
| Output load | $C_L$ (100 pF) | 1 |

**NOTE:**
1. Includes scope and jig capacitance.

## CAPACITANCE [1] ($T_A$ = 25°C, f = 1 MHz)

| PARAMETER | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| Input capacitance | $C_{IN}$ | $V_{IN}$ = 0 V | | | 7 | pF |
| I/O capacitance | $C_{I/O}$ | $V_{I/O}$ = 0 V | | | 10 | pF |

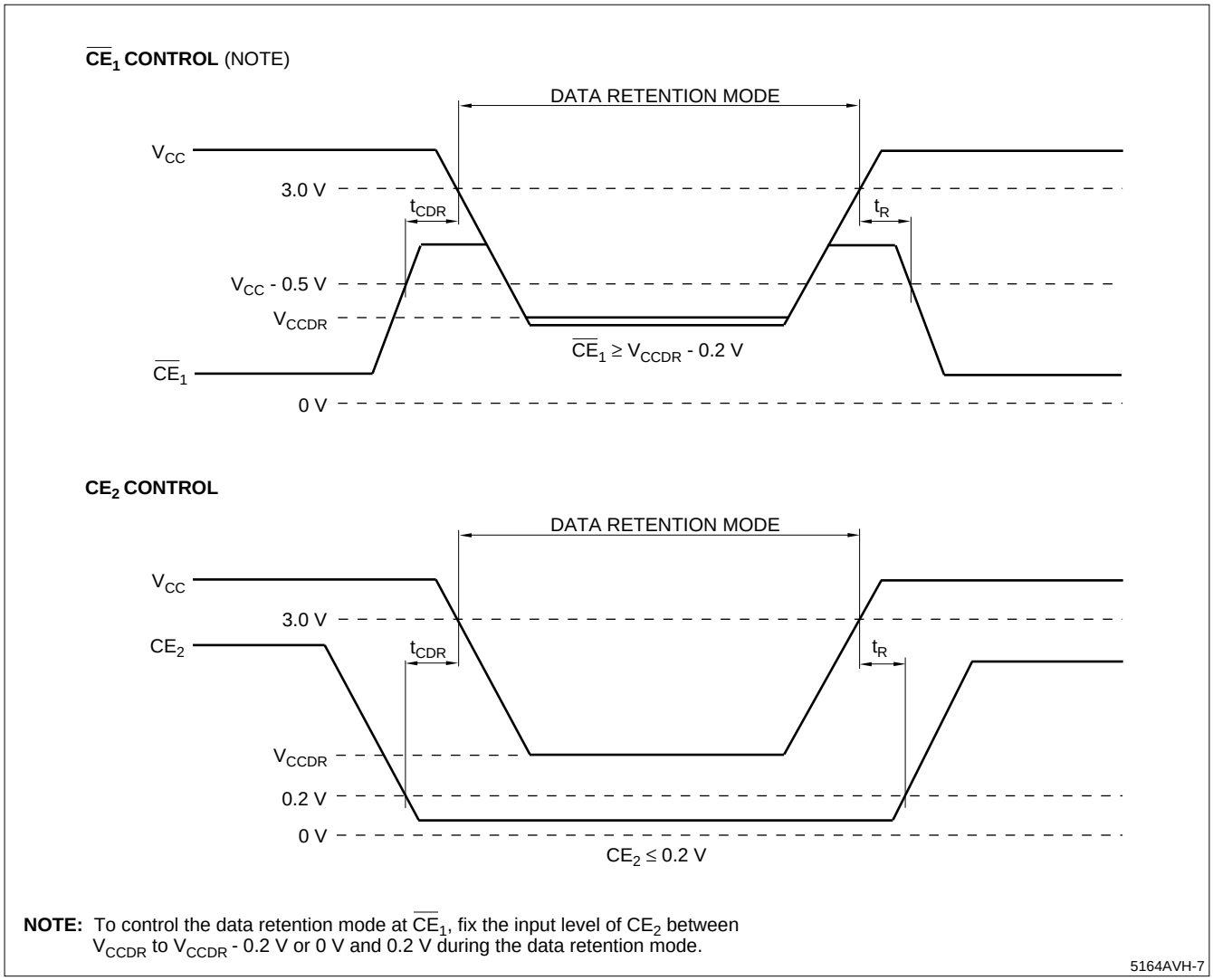
**NOTE:**
1. This parameter is sampled and not production tested.

## DATA RETENTION CHARACTERISTICS ($T_A$ = –40°C to +85°C)

| PARAMETER | SYMBOL | CONDITIONS | | MIN. | MAX. | UNIT | NOTE |
|---|---|---|---|---|---|---|---|
| Data retention supply voltage | $V_{CCDR}$ | $\overline{CE_2} \le 0.2$ V or $\overline{CE_1} \ge V_{CCDR} - 0.2$ V | | 2.0 | 5.5 | V | 1 |
| Data retention supply current | $I_{CCDR}$ | $V_{CCDR}$ = 3 V, $\overline{CE_2} \le 0.2$ V or $\overline{CE_1} \ge V_{CCDR} - 0.2$ V | $T_A$ = 25°C | | 0.2 | µA | 1 |
| | | | $T_A$ = 70°C | | 0.6 | µA | |
| | | | | | 1.5 | µA | |
| Chip disable to data retention | $t_{CDR}$ | | | 0 | | ns | |
| Recovery time | $t_R$ | | | $t_{RC}$ | | ns | 2 |

**NOTES:**

1. $\overline{CE_2}$ should be ≥ $V_{CCDR}$ – 0.2 V or ≤ 0.2 V when $\overline{CE_1} \ge V_{CCDR} - 0.2$ V.
2. $t_{RC}$ = Read cycle time.




**NOTE:** To control the data retention mode at $\overline{CE_1}$, fix the input level of $CE_2$ between $V_{CCDR}$ to $V_{CCDR}$ - 0.2 V or 0 V and 0.2 V during the data retention mode.

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**Figure 4. Data Retention Characteristics**

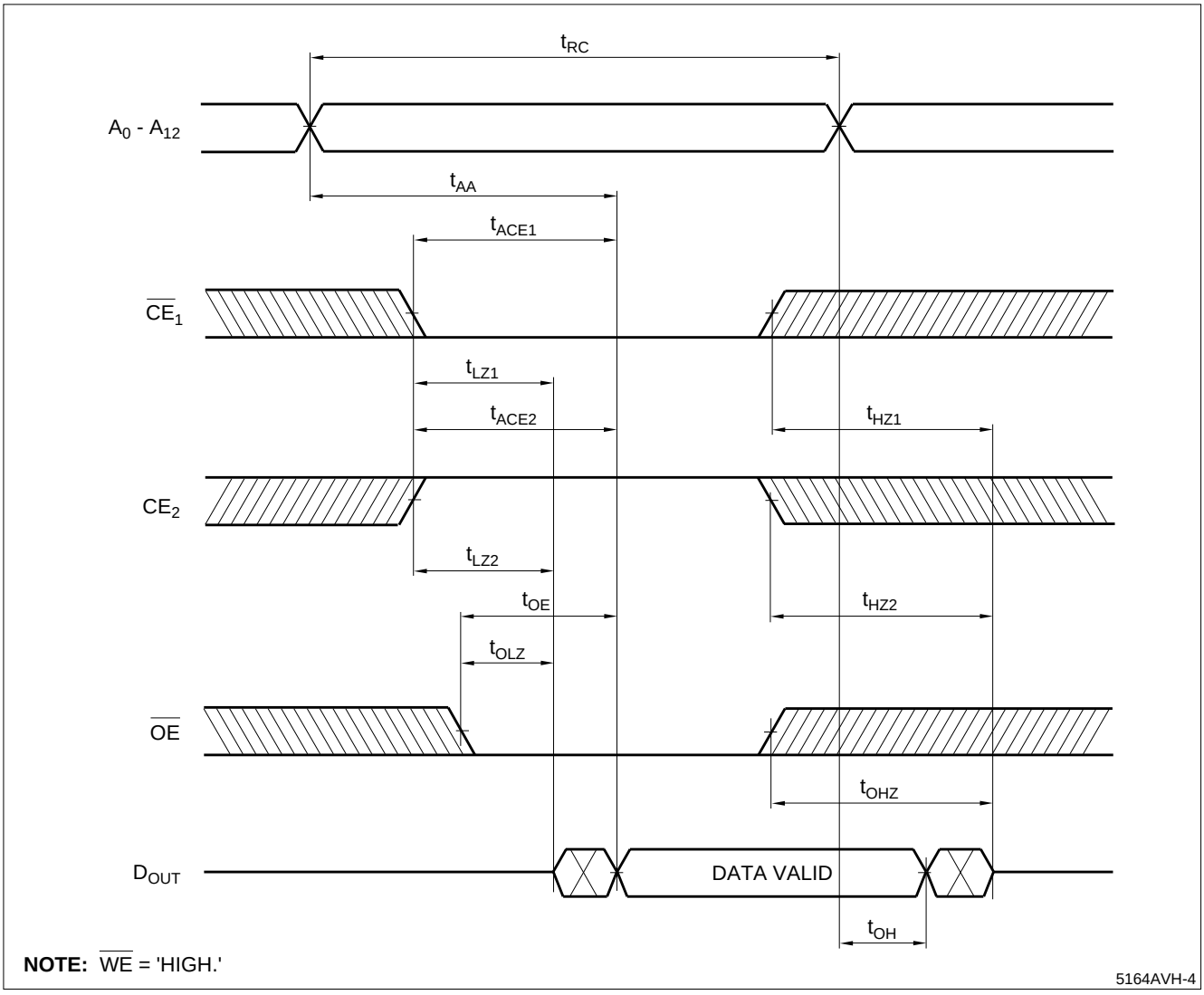
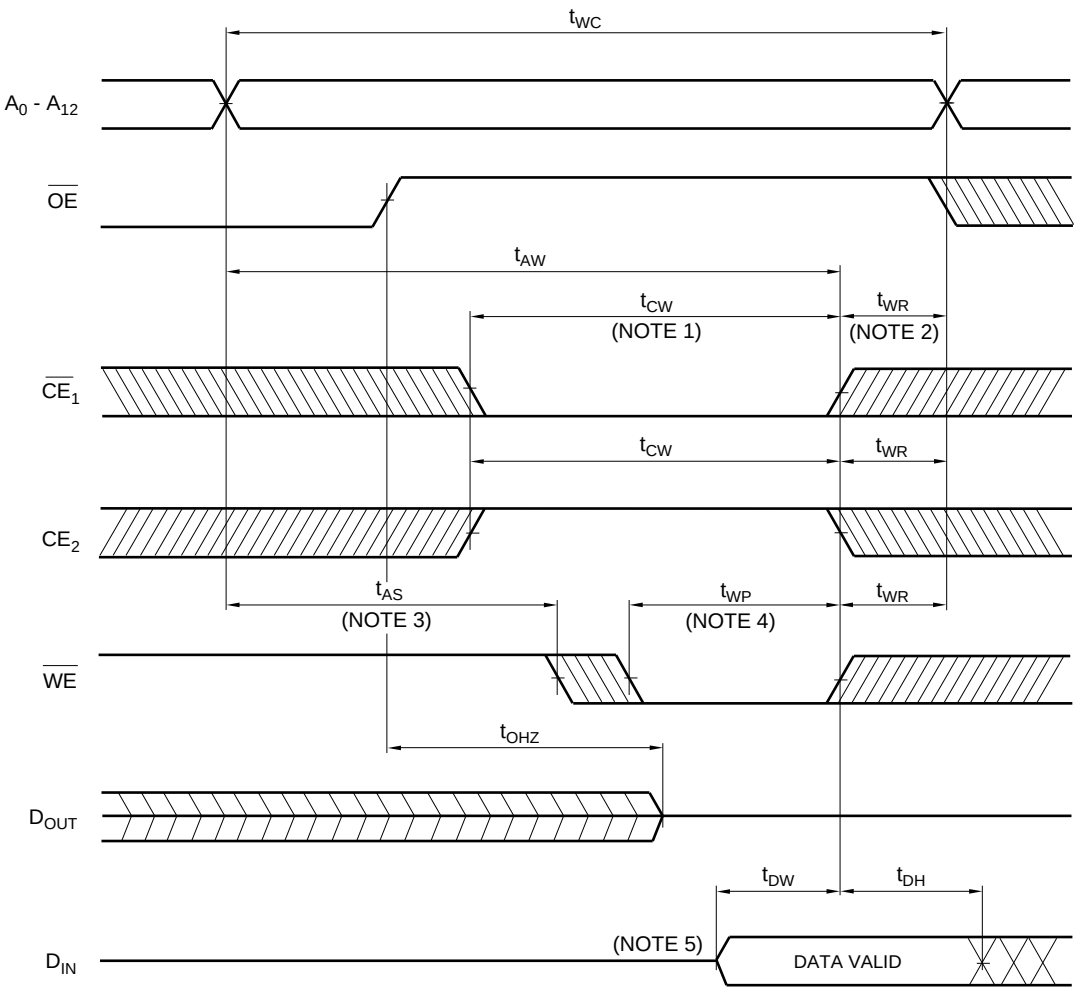



**Figure 5. Read Cycle**




**NOTES:**

1. $t_{CW}$ is defined as the time from the last occuring transition, either $\overline{CE_1}$ LOW transition or $CE_2$ HIGH transition, to the time when the writing is finished.
2. $t_{WR}$ is defined as the time from writing finish to address change.
3. $t_{AS}$ is defined as the time from address change to writing start.
4. The writing occurs during an overlapping period of $\overline{CE_1}$ = 'LOW,' $CE_2$ = 'HIGH,' and $\overline{WE}$ = 'LOW' ($t_{WP}$).
5. When I/O pins are in the output state, input signals with the opposite logic level must not be applied.

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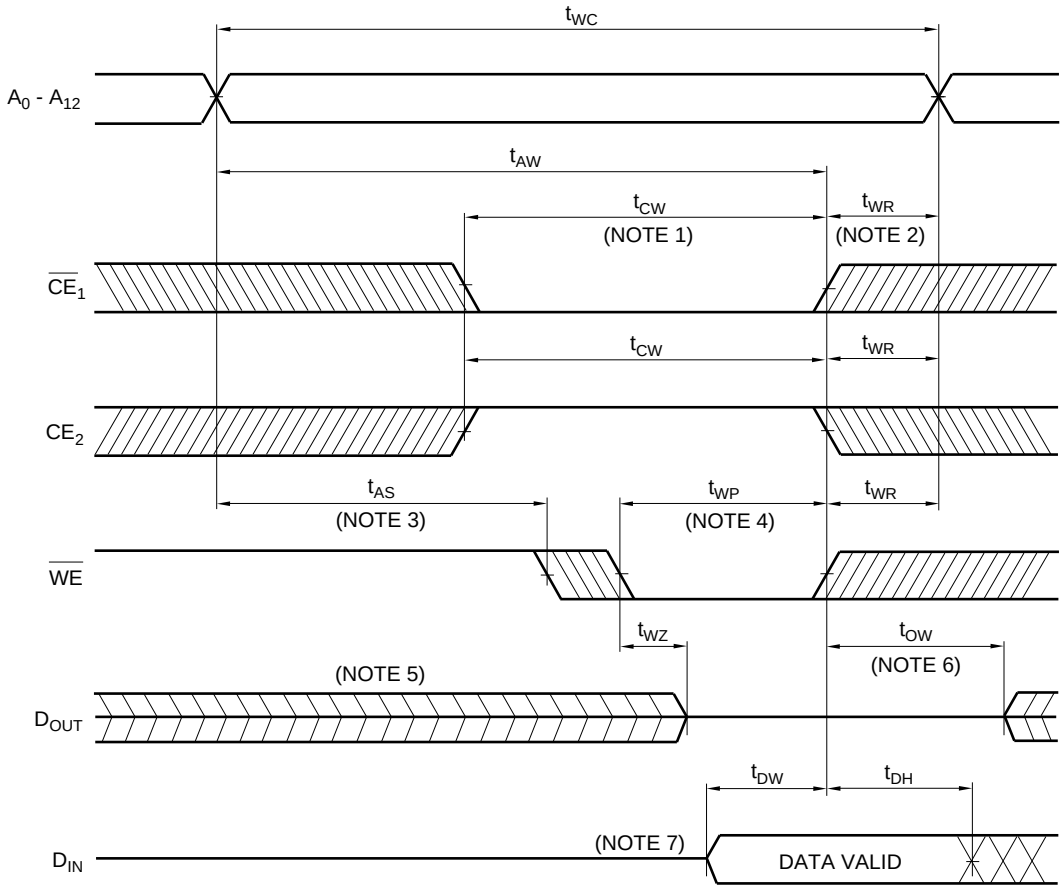
**Figure 6. Write Cycle ($\overline{OE}$ Controlled)**




**NOTES:**

1. $t_{CW}$ is defined as the time from the last occuring transition, either $\overline{CE_1}$ LOW transition or $CE_2$ HIGH transition, to the time when the writing is finished.
2. $t_{WR}$ is defined as the time from writing finish to address change.
3. $t_{AS}$ is defined as the time from address change to writing start.
4. The writing occurs during an overlapping period of $\overline{CE_1}$ = 'LOW,' $CE_2$ = 'HIGH,' and $\overline{WE}$ = 'LOW' ($t_{WP}$).
5. If $\overline{CE_1}$ LOW transition or $CE_2$ HIGH transition occurs at the same time or after $\overline{WE}$ LOW transition, the outputs will remain high-impedance.
6. If $\overline{CE_1}$ HIGH transition or $CE_2$ LOW transition occurs at the same time or before $\overline{WE}$ HIGH transition, the outputs will remain high-impedance.
7. When I/O pins are in the output state, input signals with the opposite logic level must not be applied.

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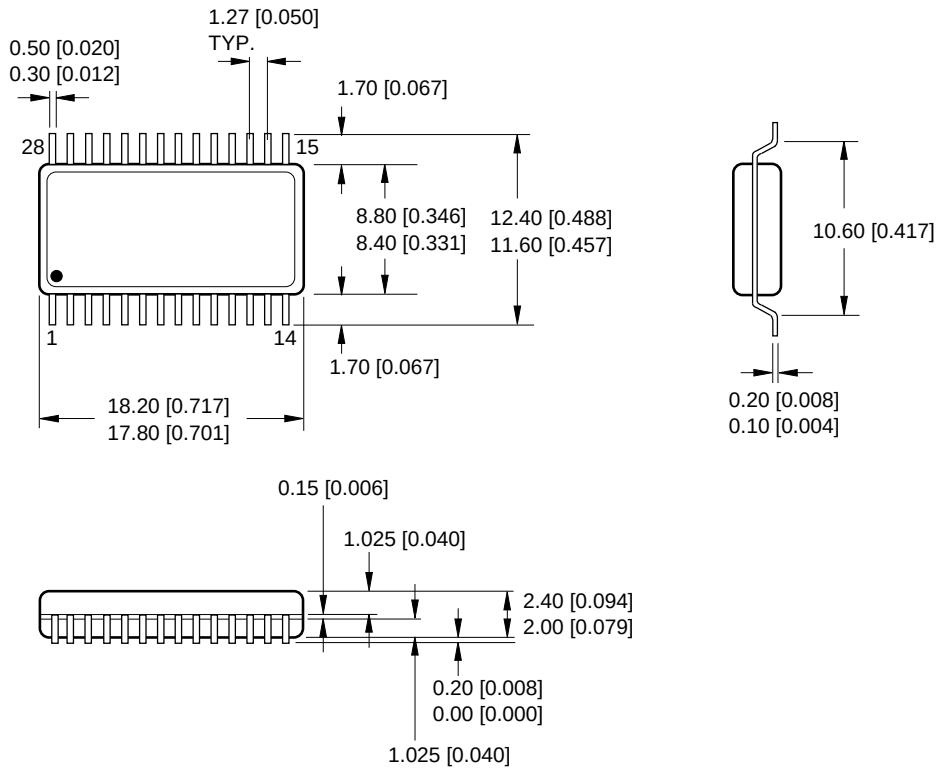
**Figure 7. Write Cycle ($\overline{OE}$ Low Fixed)**

## PACKAGE DIAGRAMS

**28SOP (SOP028-P-0450)**

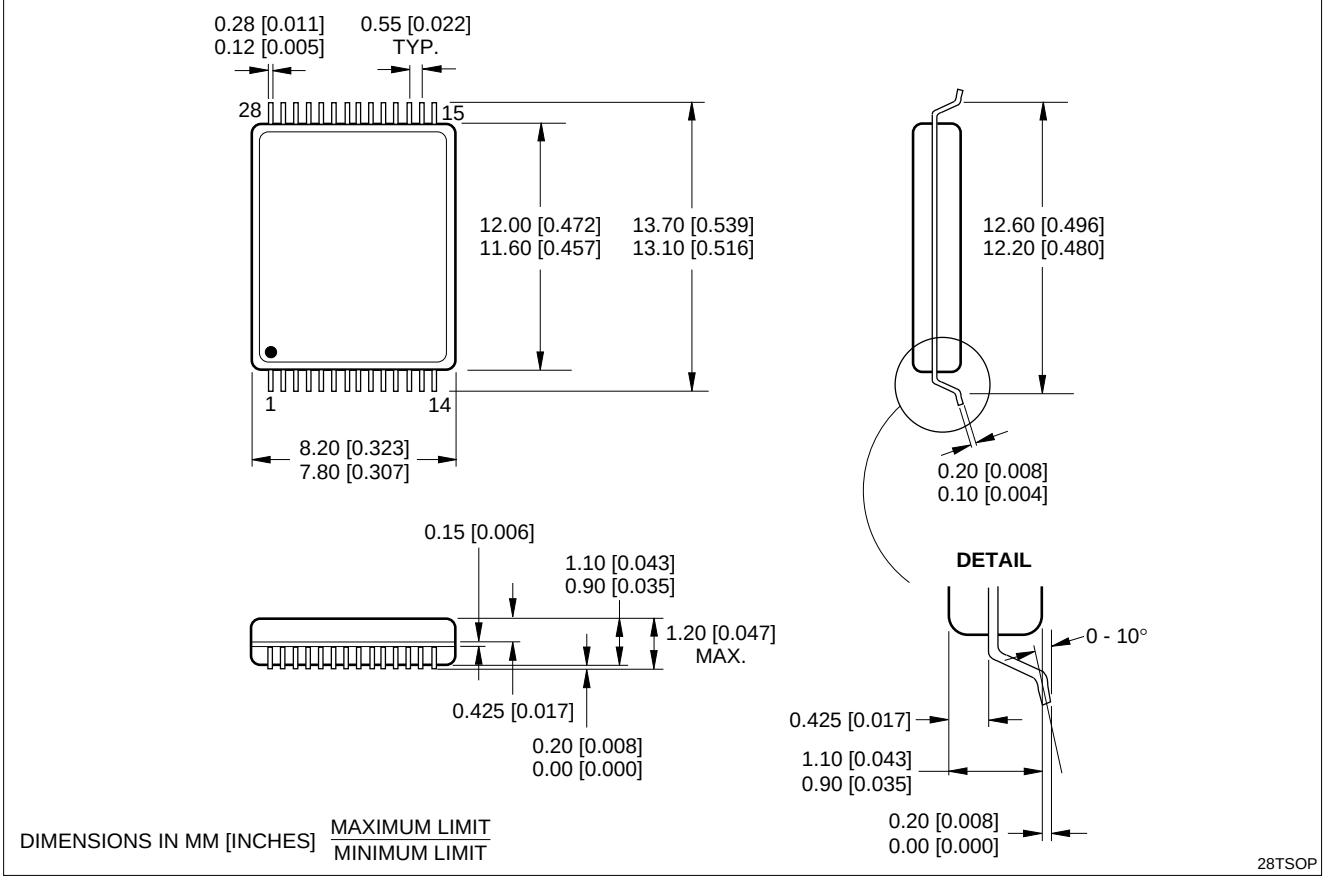



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

28SOP

**28-pin, 450-mil SOP**

**28TSOP (TSOP028-P-0813)**




**28-pin, 8 × 13 mm$^2$ TSOP (Type I)**

## ORDERING INFORMATION